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JAPANESE PATENT APPLICATION

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[0009]

[Embodiment] One embodiment of the present invention is described below with reference to the accompanying drawings. Fig. 1 shows a structure in section of a field effect transistor composed of an epitaxially grown substrate. The structure of the epitaxially grown substrate is described following the fabrication steps.

[0010] Herein, the epitaxial growth means a molecule beam epitaxial growth (MBE), but the growth may be performed by any methods such as a MOCVD (Metal Organic Chemical Vapor Deposition) method only if the methods are capable of controlling the growth in atom layer order.

[0011] First, a monocrystalline substrate 11 of a semi-insulating GaAs semiconductor is prepared, and 0.5 μ m buffer layer 12 of i-GaAs to which no impurity is doped is formed is formed on the monocrystalline substrate 11 by the epitaxial growth.

[0012] After the buffer layer 12 is grown, 300nm barrier layer 13 is formed thereon. The barrier layer 13 is made of $Al_{0.3}Ga_{0.7}As$.

[0013] After 6nm i-GaAs layer 141 to which no impurity is doped is grown on the barrier layer 13, the shutter of a Ga vaporizer, which has been opened for the growth, is closed and the shutter of a Si vaporizer is opened for 60 seconds at the same time or after a few seconds to deposit a Si doped layer 151, such that one δ doped layer is formed.

[0014] Next, the shutter of the Si vaporizer is closed again and the shutter of the

Ga vaporizer is opened to grow a 6nm i-GaAs layer 142. After the shutter of the Ga vaporizer is closed, the shutter of the Si vaporizer is opened for 60 seconds to deposit a Si doped layer 152. 5-time repetition of the above steps forms a multilayer structure in which impirty-undoped i-GaAs layers 141-145 (14) and the Si doped layers 151-155 (15) are alternately arranged. Then, an i-GaAs layer 146 is deposited thereon, thereby completing the multilayer structure.

[0015] In other words, the multilayer structure is composed of lamination of the i-GaAs layers each serving as one unit of base semiconductor layer, and a heteroatom is doped to at lease one atom layer of the base semiconductor layers in the interface of the laminated base semiconductor layers so as to form a doped layer (δ doped layer). 5 layers of the δ doped layer are formed.

[0016] On such the multilayer structure, 30nm i-$Al_{0.3}Ga_{0.7}As$ barrier layer 16 is formed, then an i-GaAs cap layer 17 is formed thereon, to thus obtain the epitaxially grown substrate.

[0017] The field effect transistor is composed using the above epixtaxially grown substrate. In detail, high frequency sputtering is first performed to form 30nm Wsi_x thin film (x=0.6) over the entirety of the surface of the epitaxially grown substrate, i.e., the surface of the cap layer 17. Then, the thus formed thin film is pattern-etched by reactive ion etching to form a gate electrode 21.

[0018] After the gate electrode 21 is formed in this way, Si ions are implanted from the surface of the cap layer 17, using the gate electrode 21 as a mask, and annealing is performed at 900℃ for 5 seconds to activate the doped Si, thereby forming n+ layers 221, 222 (doted regions surrounded by chain lines in the drawing).

[0019] Thereafter, a source electrode 23 and a drain electrode 24 are formed in such a manner that 40nm AuGe and 150nm Au are respectively deposited on a

source/drain regions respectively corresponding to the n+ layers 221, 222 on the surface of the cap layer 17 and sintering is performed at 450℃ for 90 seconds.

[0020] Fig. 2 shows a temperature dependency of the electron mobility in the epitaxially grown substrate structured as above. As cleared from the drawing, the electron mobility converges within the narrow range of 1020 to 950 cm2/Vs in the temperature range of 77K to 350K. Further, the sheet carrier density is $2 \times 10^{13} cm^{-2}$, which is larger than the case with one δ doped layer.

[0021] The above phenomena are caused by the following factors. First, the multilayer of two or more δ doped layers, instead of one δ doped layer, increases the sheet carrier density. The sheet carrier density is multiplied by the number of the layers. This enables to adequately select a value of each interval between the δ doped layers.

[0022] In this embodiment, the number of the δ doped layers is set to 5, wherein the same effects are exhibited with the two or more δ doped layers. Fig. 3 shows comparison in the temperature dependency of the electron mobility between a case with one δ doped layer and a case with two δ doped layers. It is understood that the temperature dependency is remarkably decreased in the case with two δ doped layers, compared with the case with one δ doped layer.

[0023] Each interval between the δ doped layers are set to 6nm in this embodiment, wherein the same effects are exhibited with the intervals of 100nm or narrower. The narrower the intervals are set, the more remarkable effect of two-dimensional phonon is expected. Fig. 4 shows the temperature dependencies of the sheet carrier densities in the case with one δ doped layer and in the case with two δ doped layers. Increase in number of δ doped layers attains a necessary value of the sheet carrier density.

[0024] The bandgap is different between AlGaAs and GaAs at the interface of the n-type AlGaAs layer and the GaAs layer in contact therewith, and AlGaAs has a wider bandgap. For this reason, the electrons move toward GaAs having a larger electron affinity from AlGaAs. The insulating property is enhanced as the bandgap becomes wider.

[0025] Referring to the present embodiment, the GaAs layer 14 including the δ doped layer is interposed between the AlGaAs layers 13, 16 in Fig.1 . Accordingly, the electrons are hard to enter into the AlGaAs layers 13, 16, which have the wide bandgap, with a result that the electrons are confined in the GaAs layer 14. In other words, the sheet carrier density is increased. Further, with the AlGaAs layer 16, the Schottky barrier becomes large immediately below the gate electrode 21, which result in a higher gate withstanding voltage.

[0026] Wherein, the monocrystalline substrate 11 is made of GaAs in this embodiment, but may be made of a general semiconductor such as Si, Ge, InP, as well as GaAs. Further, the impurity atoms to be δ -doped is not limited to Si exemplified in the present embodiment.

[0027] In addition, the barrier layer 13 may be dispensed with in the structure shown in Fig. 1 or the barrier layer 16 may be dispensed with. In any of these cases, the temperature characteristic is improved. Moreover, ion implantation becomes unnecessary in fabricating the field effect transistor if the i-AlGaAs layer and the i-GaAs layer respectively composing the barrier layer 16 and the cap layer 17 are n-type layers.

[0028] As described above, with the compound semiconductor device according to the present invention, a transistor applicable to a high-speed high-frequency circuit with no variation of the transistor characteristic such as electron mobility over a wide temperature range can be achieved.

[Brief Description of Drawings]

[Fig. 1] A section showing the field effect transistor composed of the compound semiconductor according to one embodiment of the present invention.

[Fig. 2] A graph explaining the temperature dependencies of the electron mobility and the sheet carrier density in the compound semiconductor exemplified in the embodiment.

[Fig. 3] A graph for comparing between a case with one δ doped layer and a case with two δ doped layers in the temperature dependency of the electron mobility.

[Fig. 4] A graph for comparing between the case with one δ doped layer and the case with two δ doped layers in the temperature dependency of the sheet carrier density.

Fig. 1

23: sour electrode 21: gate electrode 24: drain electrode

11: semi-insulating GaAs substrate

12: buffer lyaer (i-GaAs)

13: i-AlGaAs layer

14: i-GaAs layer

15: Si doped layer

16: i-AlGaAs layer (barrier layer)

17: i-GaAs layer (cap layer)

Fig. 2

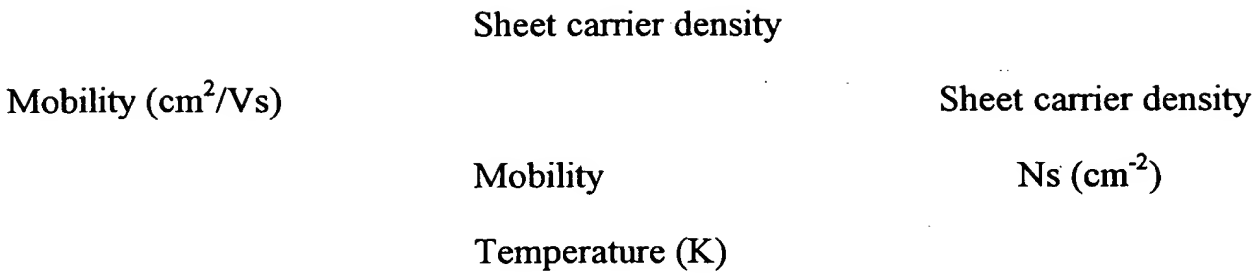

Fig. 3

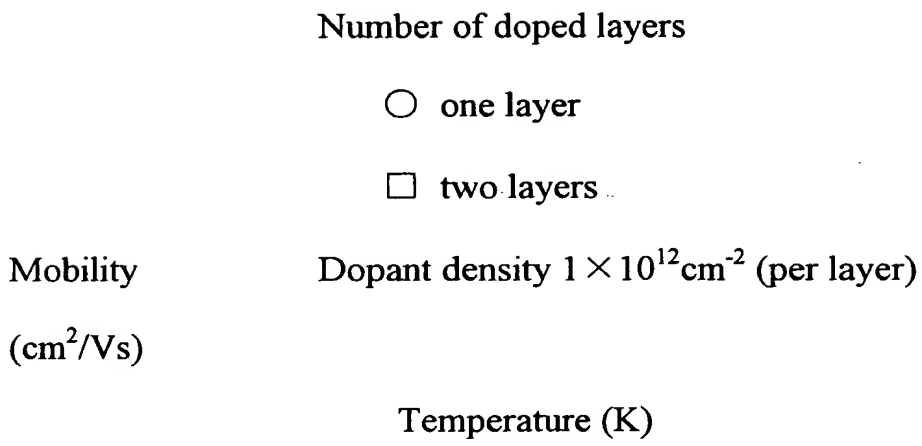

Fig. 4